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Monte Carlo simulations of AlGaN/GaN heterojunction field-effect transistors (HFETs)

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Abstract

Self-consistent Monte Carlo simulations are reported for AlGaN/GaN HFETs. Hot-carrier scattering rates are determined by fitting experimental ionization coefficients and the doping character of the GaN is obtained from substrate bias measurements. Preliminary simulations for a simple model of the AlGaN surface are described and results are found to be consistent with experimental data. The high-frequency response of short-gate-length transistors is found to be sensitive to the charge state of the free AlGaN surface and it is proposed that current-slump phenomena may also be related to deep levels at this surface. Breakdown calculations show interesting two-dimensional effects close to the drain contact.

1. Introduction

GaN is currently of great interest both for short-wavelength optoelectronics and for microwave power devices. The high breakdown field allows large voltage swings on the drain terminal of a FET and heat sinking through SiC substrates allows very high power output (>9.8 W mm^{-1} CW at X band [1]). The saturated drift velocity for electrons is thought to be higher than 10^7 cm s^{-1}, though this occurs at relatively high electric fields. High channel electron mobility (1200–1700 cm^2 V^{-1} s^{-1} [1]) is also available for high-electron-mobility transistors (HEMTs). Consequently it is possible to achieve good high-frequency performance. The observed concentration of line defects in devices fabricated on SiC is still rather high ($>10^8$ cm^{-2}) and trapping effects are also observed in the transport characteristics through current-slump phenomena. It is therefore likely that defect-related mechanisms may be masking the true potential of the material in current experimental observations. The whole field has been

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covered recently in a special issue of *IEEE Transactions on Electron Devices* [1] where the potential for microwave power devices is discussed in detail. Scaling to very short channel lengths by exploiting the high breakdown field also appears possible [2], with implications for MMIC (monolithic microwave integrated circuits) circuits at mm-wave frequencies for advanced radar and communication systems.

In the present paper we develop a Monte Carlo model for these transistors with the aim of predicting possible high-frequency performance limits. Comparison of simulation results with experimental data should also help to unravel the complex physics involved. The bulk band structure of wurtzite GaN is modelled with five conduction band valleys, with masses and non-parabolicity factors estimated from pseudopotential band structure. The Monte Carlo simulation includes impurity scattering and all of the standard phonon scattering processes. It also allows for alloy scattering and piezoelectric scattering. The polar optic phonon scattering dominates at low energy within the Γ valley and is calculated from the Frohlich coupling. To model the transport at high energy we note that impact ionization is very sensitive to carrier heating and phonon scattering. We accordingly scale the inter-valley scattering rates to fit measured ionization coefficients. The resulting model of bulk transport is then used to model AlGaN/GaN HEMTs. For this 2D transistor modelling we use the SLURPS (Subroutine Library: Universal Random Particle Simulator) self-consistent Monte Carlo simulation software which has been developed in the Physics Department at Durham University over a number of years[5].

In section 2 we discuss bulk transport in detail and compare simulations with experimental data where available, and with results from other authors. The resulting parameter set has been used with SLURPS to model GaN HEMTs as described in section 3. The strained AlGaN barrier layer has a piezoelectric charge at the GaN/AlGaN interface, which is modelled as a thin sheet of ionized donors. The GaN is taken to be p-type with acceptor concentration derived from substrate bias measurements [3]. In section 3, simulations of I_d–V_g characteristics are also compared with experimental measurements, and we present some preliminary results for a model of trapping at the AlGaN surface. In section 4 we consider the high-frequency performance of the transistors and its dependence on the charge state of the free AlGaN surface. Finally in section 5 we consider the breakdown properties of the transistors.

2. Bulk transport

Hot-electron transport in wurtzite GaN involves a number of valleys and the inter-valley scattering rates are at present unknown. In order to set realistic values, we initially used a 1D Monte Carlo model with two valleys, and adjusted the high-energy scattering rates to achieve agreement with measured electron impact ionization rates [4]. The ionization scattering rate was taken in the Keldysh form, using Si parameters [15] with an increased band gap. It should be noted that the measured ionization rates are more sensitive to carrier heating and electron–phonon interactions than to the ionization scattering cross sections, so this procedure is considered adequate at this stage. A comparison of theory and experiment is shown in figure 1. The SLURPS software does not include the impact ionization process at present, so the inter-valley scattering potential in SLURPS was adjusted to obtain agreement with the mean carrier energy (W) as a function of electric field. The resulting plot of W at room temperature is shown in figure 2 and the velocity–field curves are shown in figure 3. The room temperature peak velocity of 2.5×10^7 cm s^{-1} is rather high compared with the measured values by Wraback *et al* [5] of 1.8×10^7 cm s^{-1}, which may indicate that defect scattering

[5] Details are available from Professor R A Abram.

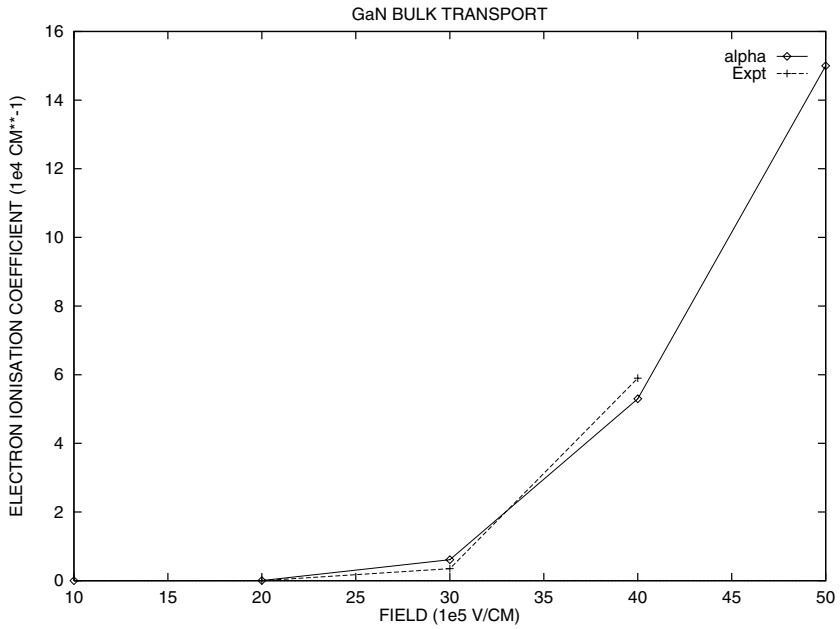

Figure 1. Comparison of theory and experiment for the electron ionization coefficient in GaN. This comparison is used to determine the inter-valley electron–phonon scattering rates.

Table 1. Wurtzite GaN material parameters. Note: dielectric constants: $\varepsilon_0 = 9.5$, $\varepsilon_\infty = 5.35$; density ρ (kg m^{-3}): 6150; sound velocity (m s^{-1}): 4330; acoustic deformation potential (eV): 8.3; piezoelectric constant (Cm^{-2}): 0.375; polar optic phonon energy (eV): 0.0995; lattice constant (Å): 3.189; Schottky barrier height (eV): 1.0.

Valley	E (eV)	m^* (parallel)	m^* (perpendicular)	Nonparabolicity (eV^{-1})
Γ	0.0	0.2	0.18	0.189
U	1.0	0.4	0.4	0.065
Γ_3	1.1	0.6	0.6	0.029
M	2.0	0.57	0.57	0.0
K	2.1	0.3	0.3	0.7

processes are present which are not represented in the Monte Carlo simulation. The room temperature velocity–field curve in figure 3 is in quite good agreement with other published Monte Carlo results [6–8].

Experimental studies of hot-electron dynamics using femtosecond optical pulses [9] indicate that the Γ–U separation is 1.34 eV. We found a good fit to measured ionization coefficients by setting this energy separation at 1.0 eV. The band parameters used in the FET simulations are shown in table 1.

The energy balance approach provides an interesting alternative to Monte Carlo simulation for hot-carrier transport. This technique computes the mean electron energy, and because it is computationally fast compared to Monte Carlo simulation, it is attractive as an engineering tool for device design. The technique is also available in commercial simulators. Monte Carlo simulation can provide the relaxation times required for this approach and we present results

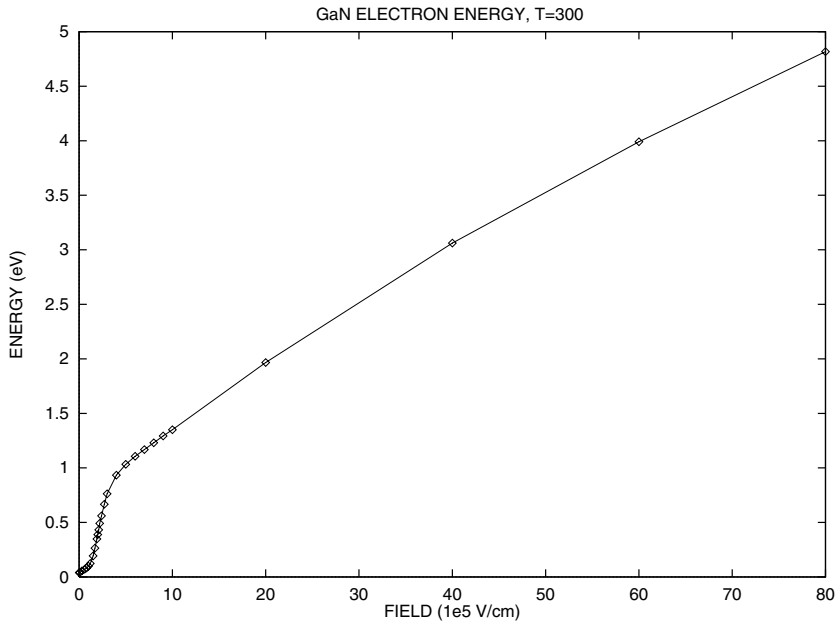

Figure 2. Mean electron kinetic energy versus electric field, using inter-valley scattering rates adjusted to fit experimental ionization coefficients.

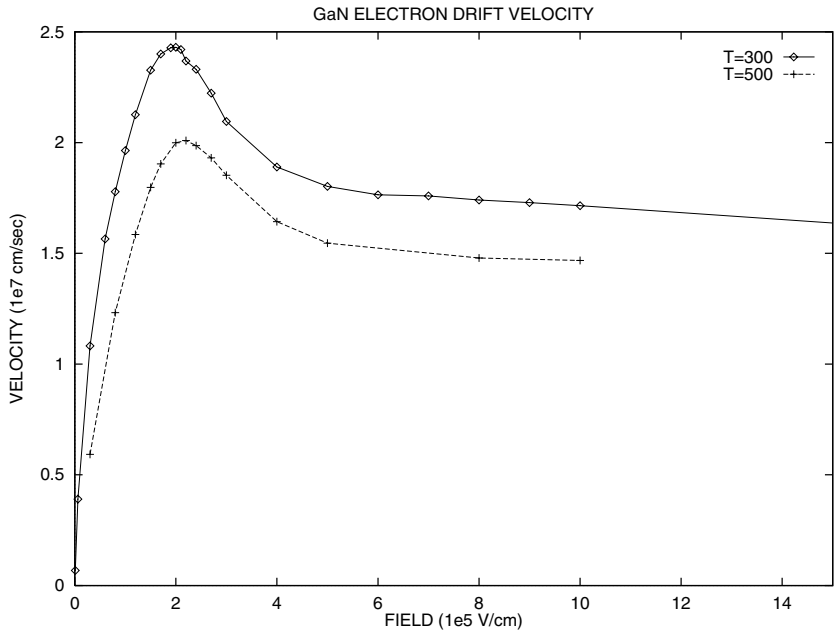

Figure 3. The electron drift velocity for GaN at two lattice temperatures and a range of electric fields.

for GaN here. The energy balance equations for a spatially uniform system can be defined as

$$\frac{\mathrm{d}W}{\mathrm{d}t} = qFV(F) - \frac{W - W_0}{\tau_E} \tag{1}$$

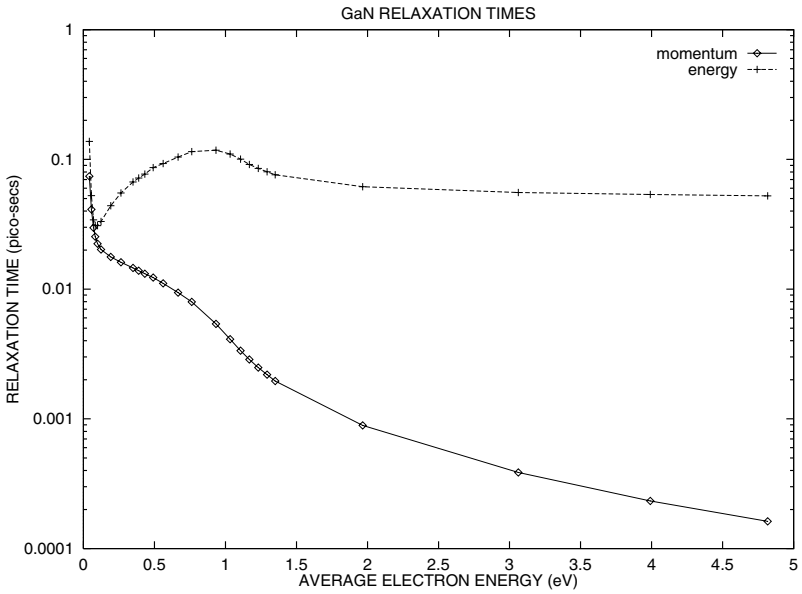

Figure 4. Energy and momentum relaxation times obtained from Monte Carlo energy and drift velocity calculations. The momentum relaxation time was obtained using an effective mass of 0.2. The energy relaxation time is independent of m^*.

$$\frac{\mathrm{d}[m^*V(F)]}{\mathrm{d}t} = qF - \frac{m^*V(F)}{\tau_P} \tag{2}$$

where q is electronic charge, $V(F)$ is the electron drift velocity, F is the applied electric field, W_0 is the thermal energy, m^* is the average effective mass, τ_E is the energy relaxation time, τ_p is the momentum relaxation time and W is the mean carrier energy. In principle m^* is a function of W, but this complication is usually ignored in commercial simulators, except through a parametrized velocity–field characteristic. Equations (1) and (2) are readily solved for the relaxation time at a given value for F [10], and in the steady state the relaxation times can be expressed in the form

$$\tau_p = \frac{m^*V(F)}{qF} \qquad \tau_E = \frac{(W - W_0)m^*}{q^2F^2\tau_P}. \tag{3}$$

To obtain numerical values, the velocity–field curve was first obtained from Monte Carlo simulation, when τ_p is obtained immediately as a function of F. The $W(F)$ curve is also obtained from Monte Carlo simulation and, together with $\tau_p(F)$, yields $\tau_E(F)$ from (3). From the curve for $W(F)$, the relaxation times τ_p and τ_E can then be obtained as functions of W. The results from SLURPS are shown in figure 4. The value for τ_E is considerably smaller than the value obtained by Foutz *et al* [10] which reflects the stronger inter-valley scattering required to fit the measured ionization coefficients.

3. HFET model

The transport parameters for bulk GaN described in section 2 were used with the SLURPS software to develop a model for the AlGaN/GaN HFET. We have concentrated on AlGaN with an aluminium fraction of 24% in this work and the geometry of the SLURPS model is shown in

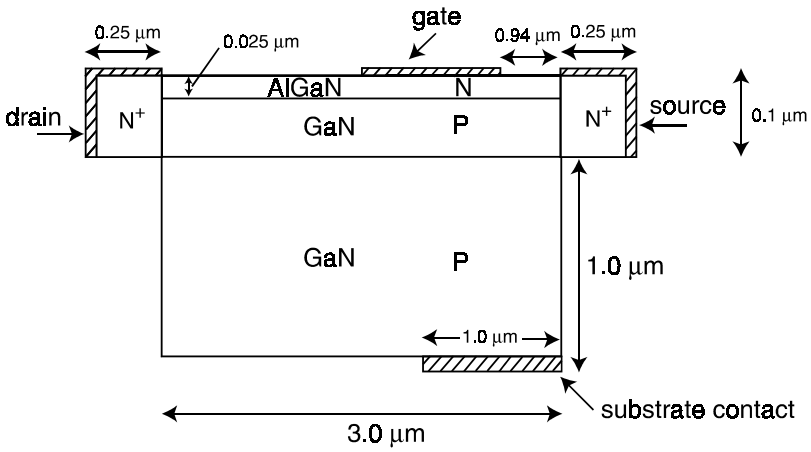

Figure 5. The geometry of the Monte Carlo transistor model. This geometry corresponds closely to the experimental devices used for comparison.

figure 5. From substrate bias measurements we know that for GaN grown on SiC, the GaN is p-type with a net hole density of 1.6×10^{17} cm^{-3} [3]. The GaN also has weak n-type conductivity with the Fermi level about 0.9 eV below the conduction band edge [3]. This can be modelled by assuming a deep acceptor with energy 0.9 eV below the conduction band edge and a low density of shallow donors. Some of the donor electrons recombine with holes in the acceptor impurity band causing the Fermi level to pin within this band, and the remaining donor electrons populate the conduction band at a density determined by the pinned Fermi level. The time constants for the hole population to adjust to changing substrate bias are around 1 s, which is far too long to be modelled by Monte Carlo simulation. To avoid this difficulty we have reduced the band gap of GaN to 1.0 eV and replaced the deep acceptor holes by free holes within the valence band. This allows the depletion layers to form correctly for the steady state, but some caution is needed for interpreting transient currents which involve holes. To treat the AlGaN/GaN heterojunction, the band gap of the AlGaN was also reduced in order to maintain the 60/40 band offsets.

The channel in the HFET is formed in response to the piezoelectric charge (Q_p) at the AlGaN/GaN interface [12]. This charge is modelled as a sheet of ionized donors placed at the interface, and the concentration is chosen as 1.56×10^{13} cm^{-2} to obtain approximate agreement with the measured pinch-off voltage. The surface of the AlGaN must have a compensating polarization charge ($-Q_p$) and in the first calculations we assumed that this surface polarization charge is neutralized, either by holes in very deep trap states or by ions introduced in the processing. We consider ways of relaxing this neutral-surface assumption later.

The geometry used for the SLURPS transistor model is shown in figure 5. The AlGaN layer is 0.025 μm thick and the source-to-drain spacing is 3.0 μm. The experimental transistors chosen for comparison had AlGaN layers which were 0.03 μm thick. This implies that our value for Q_p obtained by fitting the pinch-off voltage is about 20% too high. A gate-to-source spacing of 0.94 μm is also used. The AlGaN and 0.075 μm of GaN, together making a total thickness of 0.1 μm, was modelled with a fine mesh. In practice this layer was found to contain most of the channel electrons. A further layer of GaN with 1.0 μm thickness was modelled with a coarse mesh. The main purpose of this layer is to allow the depletion region, adjacent to the channel, to form correctly. We found that with no p contact to the GaN buffer, an instability developed in the Monte Carlo simulation, such that the potential of the floating p layer increased indefinitely. SLURPS allows holes to exit the system through the source,

drain and gate contacts, but contains no generation–recombination mechanism to re-introduce holes to form a dynamic equilibrium. To overcome this difficulty, we used an ohmic contact to the GaN for 1 μm at the source end of the buffer, with applied potential equal to the source potential. The n^+ drain and source contact regions were doped at 3×10^{18} cm^{-3} and extended for 0.25 μm beyond the channel. The AlGaN layer was arbitrarily doped n-type with a low concentration of 10^{16} cm^{-3}.

In figure 6(a) we show experimental data for two transistors. The transistor layer structures were grown by MOVPE in a close-coupled showerhead reactor with 30 nm of $Al_{0.23}Ga_{0.67}N$ on 1.2 μm of GaN. The 0.23 μm gate transistor was grown on sapphire and passivated with silicon nitride. This transistor was chosen as it shows only small current-slump effects and has good high-frequency performance. The 1 μm gate transistor was grown on SiC and was not passivated. This transistor was chosen to illustrate the large current-slump effects which can occur in this material system. The data were obtained by using microsecond electrical pulses starting from various quiescent bias points. These bias points are chosen such that there is no quiescent power dissipation and consequently no significant self-heating during the measurements. In the presence of current slump, long recovery times are observed, so the quiescent-bias-point-induced trapped charge is frozen on the timescale of the pulsed measurements. Both hot-carrier effects and tunnelling from deep states can occur at high bias and can lead to trap charging effects. Consequently it is expected that the curves obtained from the low-bias ($V_{ds} = 0$, $V_{gs} = 0$) quiescent point will involve minimal trapping and should approach the values expected in the absence of current-slump effects. From figure 6(a) it is seen that the curves from the high-bias ($V_{ds} = 20$, $V_{gs} = -5$) quiescent state show small current slump for the 0.2 μm gate passivated transistor, and a large current slump for the unpassivated 1.0 μm gate device, consistent with the model where current slump is associated with trapping at the AlGaN surface.

A comparison of theory and experiment, assuming a neutral AlGaN surface, is shown in figure 6(b) for the (0, 0) quiescent bias point. A drain-to-source bias of 20 V was chosen to saturate the drain current, and the small reduction in slope of the experimental curves relative to the theoretical values at the higher drain currents is thought to be caused by contact resistance and gate de-biasing. The pulsed measurements should minimize heating effects and it is seen that good qualitative agreement is obtained, although the theoretical drain currents are a factor of 2–3 too high.

We noted in section 2 that the Monte Carlo velocities close to the peak velocity are rather high compared with the time-of-flight measurements, suggesting that there may be scattering from defects which has not been allowed for in the simulations. Such scattering would also reduce the low-field mobility and could reduce both the drain current and f_T. This, together with a high value for Q_p, could give a reduction by a factor of about 0.6 for I_d. The remaining difference between the theoretical and experimental drain currents observed for measurements taken from the ($V_{ds} = 0$, $V_{gs} = 0$) quiescent bias could be caused by contact resistance. It is also possible that trapping at the AlGaN surface could be affecting the channel charge and reducing the current for devices exhibiting current slump [12].

The treatment of trapping in Monte Carlo is problematic because of the large time constants involved. A typical Monte Carlo simulation represents about 10^{-10} s, so events that require longer timescales are difficult to include. The dc state can be allowed for by artificially speeding up the trap processes and, in this work, the deep acceptors in the GaN buffer are allowed for by reducing the band gap of the GaN and treating the holes in the deep acceptor states as free holes within the valence band. A similar trick can be used for acceptor traps at the AlGaN surface. To simulate pulsed data, we can first establish the dc state at the quiescent bias point. If the trapped holes can respond on the timescales of the pulsed measurement, then the holes

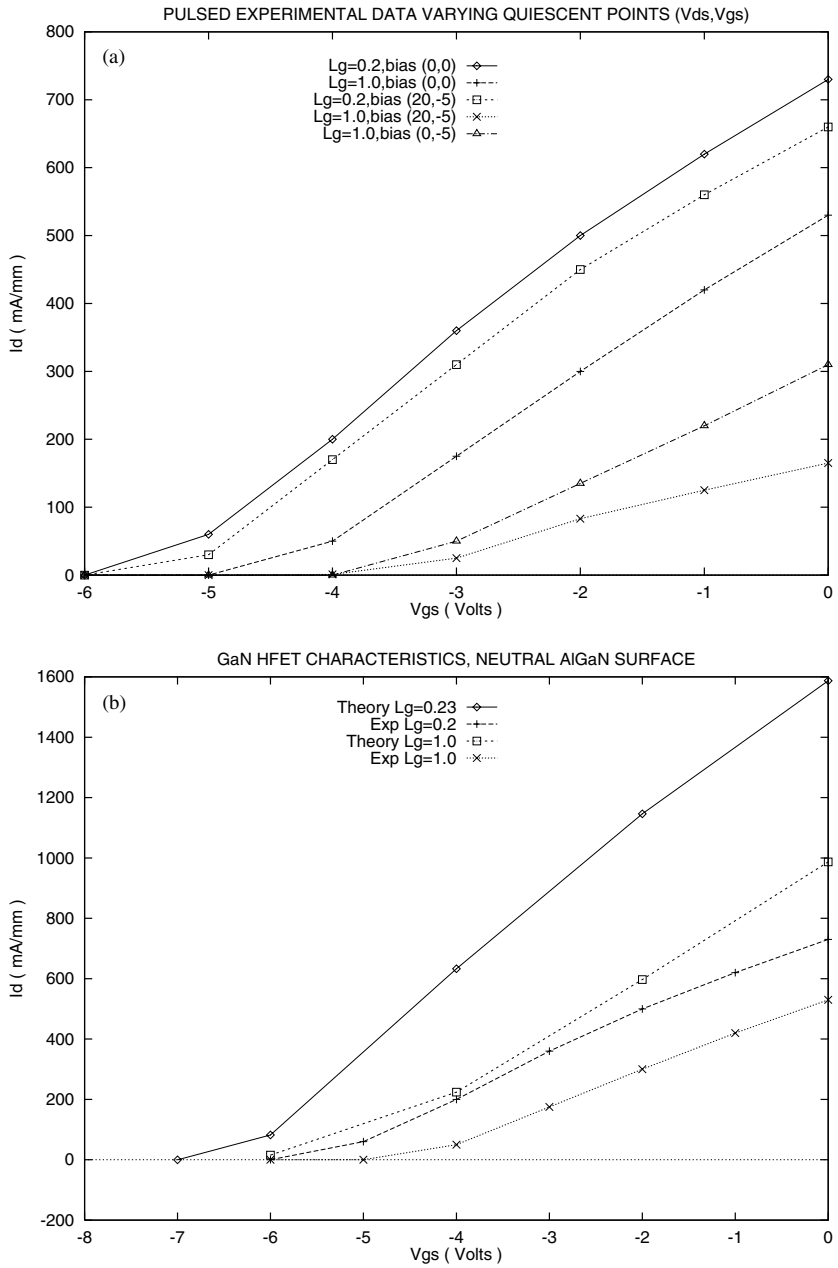

Figure 6. (a) Experimental measurements of I_d against V_g obtained for pulses (0.1 μs pulse length, 0.1% duty cycle) from various quiescent bias points. The 0.2 μm gate transistor was passivated and shows only a small current slump. The 1.0 μm gate transistor was not passivated and was chosen to illustrate the large current-slump effects which can be observed. The quiescent bias points (V_{ds}, V_{gs}) are indicated on the plots. (b) Comparison of theory and experiment for two transistor structures. The experimental devices were fabricated at QinetiQ (1 μm) and Marconi optical components (0.2 μm) [17]. This calculation assumed that the AlGaN surface was charge neutral ($Q_{sp} = 0$). The drain bias was 20 V for these results and the experimental measurements were pulsed from the ($V_{ds} = 0$, $V_{gs} = 0$) quiescent bias in order to reduce heating and minimize trapping effects.

can be regarded as mobile. If this is not the case, then the charge state of the traps can be conveniently frozen at the quiescent bias point by setting the hole mass in the AlGaN to very high values before changing the bias to represent the pulsed measurement. We are currently investigating this latter approach. Preliminary results are presented in this paper and detailed results, when available, will be presented in a later publication.

We found that the model in which trapped holes are mobile on the microsecond timescales of the pulsed experiments could simultaneously reduce both I_d and f_T, thus yielding much closer agreement with experiment. If the surface trap density (Q_{sp}) was specified in terms of the polarization charge (Q_p), then we found that values of Q_{sp}/Q_p of 0.52 and 0.41 were required for the 0.2 and 1.0 μm gate transistors respectively as shown in figure 8. This model would, however, imply a weak surface conductivity, and our measurements of surface leakage on one test wafer appeared to rule out this possibility. We therefore conclude that for the 0.2 μm gate device, with only small current slump, the high Monte Carlo velocities are probably largely responsible for the high theoretical values of I_d and f_T with contact resistance effects becoming significant at the higher values of I_d. The physical reason would be high levels of defect scattering in the material, which is neglected in the Monte Carlo model. Improvements in material quality could therefore be expected to yield a factor-of-two improvement in the high-frequency performance as indicated in figure 12(a).

To study current slump, we require to model trapping at the AlGaN surface in which the trap charge state is established at the quiescent bias point and then frozen during the pulsed measurement. As a first attempt we assume that only a fraction of the surface polarization charge is neutralized. The remaining charge, which we denote as Q_{sp}, is assumed to act as deep acceptors from which the holes can move, either by tunnelling or by emission and recapture, but with large time constants. Reasonable values for Q_{sp}/Q_p should be less than one. The high electric field between the gate and drain will deplete the holes leaving a net negative charge, which may correspond to the charging of a second virtual gate as proposed by Vetury *et al* [12]. The potential profile between the gate and source is also strongly affected, as the surface holes set the Fermi level close to the acceptor trap level, as modelled by the reduced AlGaN band gap. Q_{sp} is modelled as a sheet of acceptors at the AlGaN surface, and in figure 7 we show the theoretical variation of drain current with Q_{sp} for the two example transistors. This simulation used $V_{gs} = -2$ V and $V_{ds} = 20$ V and is valid for the dc state. In principle, Q_{sp} can be chosen to bring the theoretical drain currents into approximate agreement with experiment.

Figure 8(a) shows some results obtained with the frozen-hole model for the 0.23 μm gate transistor. It is seen that $Q_{sp} = 0.6$ actually increases the drain current by a small amount for the (0, 0) quiescent bias. A sizable reduction of I_d is also produced at the (20, -5) quiescent bias. The model is therefore capable of explaining current-slump effects. The results also confirm that the (0, 0) quiescent bias leads to I_d–V_g characteristics which are close to those expected in the absence of trapping. It is noticeable that the trapping effects reduce the slope of the curves relative to the neutral-surface ($Q_{sp} = 0$) result. Figure 8(b) shows similar results for the 1.0 μm gate transistor. In this case we have included a calculation for $Q_{sp} = 1.0$, to see the maximum slump effect obtainable from the model. It is observed that a very large effect is obtained for the (20, -5) quiescent bias, with a negligible effect for the (0, 0) quiescent bias. The model therefore looks very promising as an explanation of current-slump phenomena.

In figure 9(a) we show a contour plot of the conduction band edge for the $L_g = 0.23$ μm transistor in a dc state with $Q_{sp}/Q_p = 0.52$. The plot only includes the 0.1 μm region with the fine mesh. The source is located at $x = 0$ and the drain at $x = 3.25$ μm. The gate is located at $y = 0$, beginning at $x = 0.965$ μm. A dominant feature is the sharp drop in potential at

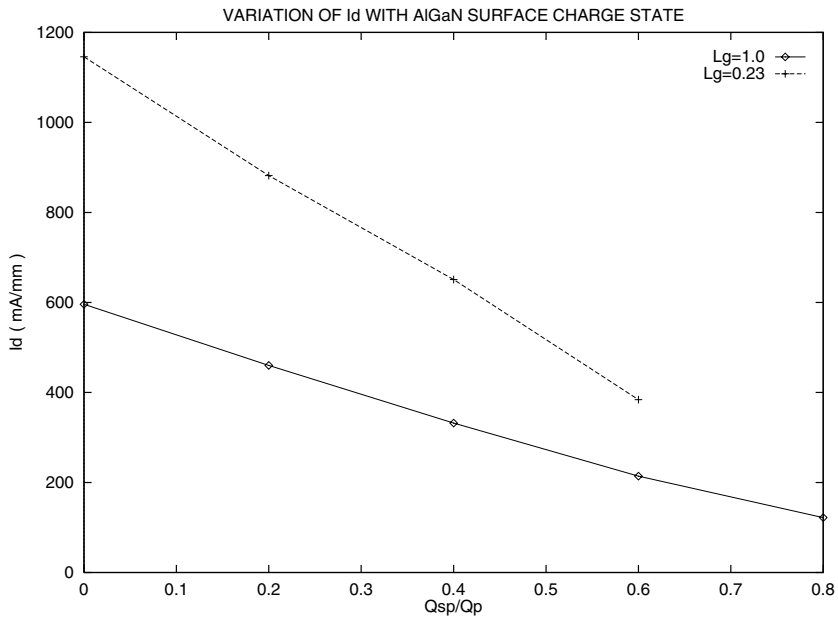

Figure 7. The variation of the modelled drain current with the surface charge, Q_{sp}. The bias conditions were $V_g = -2$ V, $V_d = 20$ V, and the transistors correspond to those of figure 6.

the drain edge of the gate. This potential drop generates hot carriers which can diffuse into the AlGaN and through the GaN towards the substrate, and may be a source of trapping. For comparison, figure 9(b) shows results for $Q_{sp} = 0$. It is seen that the presence of Q_{sp} reduces the sharp potential drop seen in figure 9(b) and also strongly affects the potential between source and gate, forcing carriers out of the AlGaN layer. In figure 10 we show the electron mean kinetic energy distribution corresponding to the case of figure 9(a). It is seen that mean energies approaching 2 eV are generated at the drain end of the gate. This energy greatly exceeds the heterojunction conduction band offset and, due to the very strong randomizing scattering, the carriers can diffuse into the AlGaN. These hot carriers may well be involved in the current-slump phenomena and would provide one mechanism for changing the charge state of the surface under high-bias conditions, either through recombination with trapped holes, or simply through electrons becoming trapped in deep states. The diffusion of hot carriers is further illustrated in figure 11 which shows the electron-density profile. This density is high at $x < 0.25$ and $x > 3.25$ μm, which correspond to the source and drain contact layers respectively. The AlGaN layer begins at $y = 0$ between the contact doping layers and has low electron density. A well defined channel layer is shown beginning at the AlGaN/GaN interface. At the drain edge of the gate, two spurs of electron charge are seen, one in the AlGaN layer extending all the way to the surface and the other extending a short distance towards the substrate. These spurs are caused by the hot-electron diffusion.

4. High-frequency performance

To study the high-frequency performance of the transistors, we first established the dc current state. Two initial simulations were performed using 40 000 particles and 20 000 particles respectively and, by comparison, it was determined that 20 000 particles were adequate to

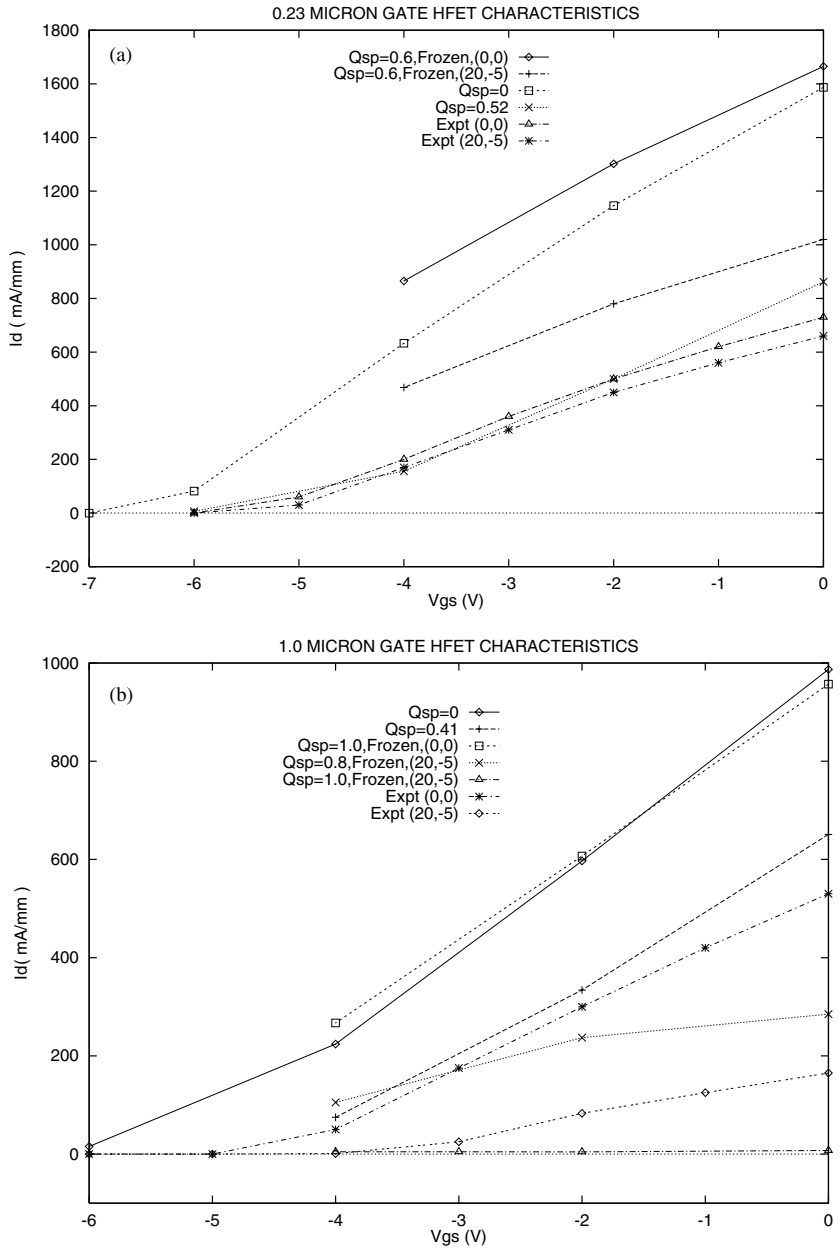

Figure 8. (a) Comparison of theory for the 0.23 μm gate transistor with pulsed experiments for the 0.2 μm gate transistor of figure 6(a). Results obtained with the frozen-hole model are labelled 'Frozen'. Other results were obtained with the mobile-hole model. The quiescent bias points (V_{ds}, V_{gs}) are labelled. (b) Comparison of theory and experiment for the 1.0 μm gate transistor of figure 6(a). Results obtained with the frozen-hole model are labelled 'Frozen'. Other results were obtained with the mobile-hole model. The quiescent bias points (V_{ds}, V_{gs}) are labelled.

model the transistors. When the dc terminal currents were stable, we applied a small-signal ac voltage pulse to the gate of the transistor and recorded the terminal currents. Following

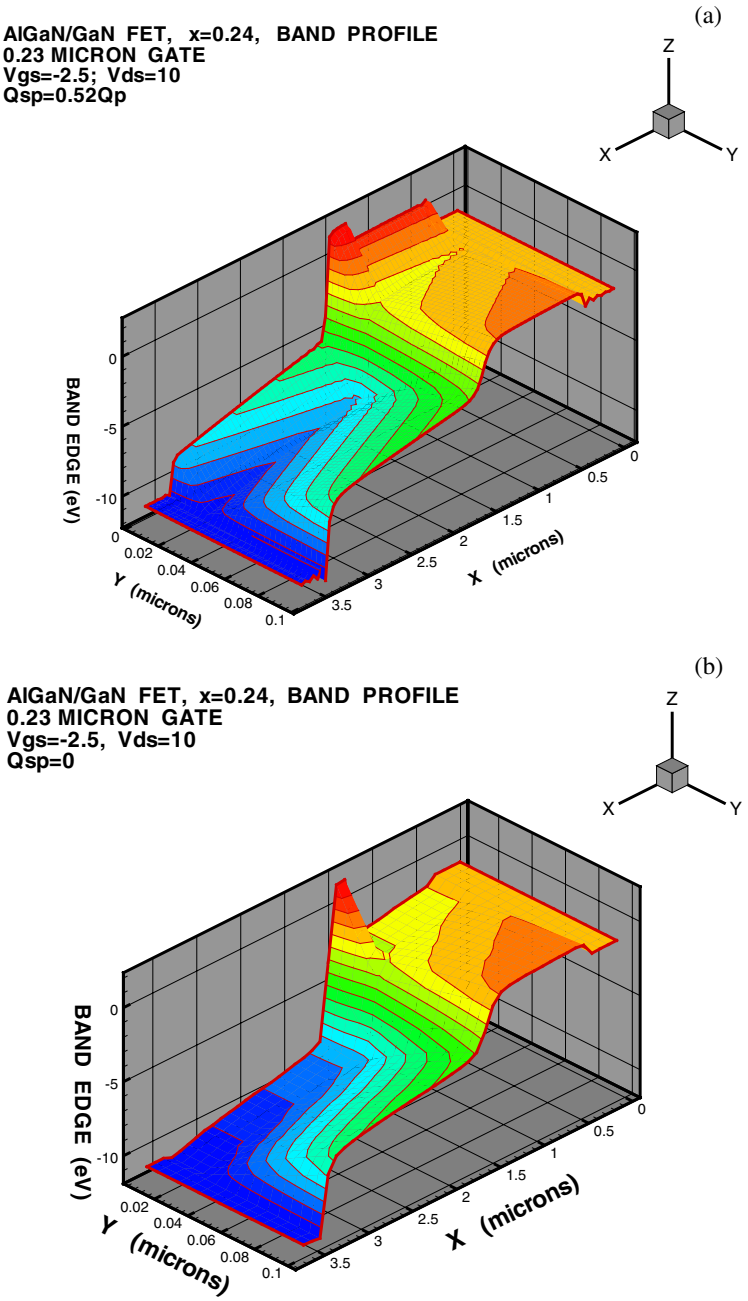

Figure 9. (a) The conduction band profile for the 0.23 μm gate transistor assuming $Q_{sp} = 0.52Q_p$. The x-axis refers to the distance from source to drain, and the y-axis refers to the distance from the AlGaN surface towards the substrate. The lines on the plot are contours of constant potential energy. The source doping layer is located at $x < 0.25$ μm and the drain doping layer at $x > 3.25$ μm as indicated in figure 5. The AlGaN layer starts at $y = 0$ and lies between the source and drain contact layers as shown in figure 5. Q_{sp} has a strong effect on the potential profile between source and gate and also reduces the potential drop at the drain edge of the gate. The bias conditions are $V_{gs} = -2.5$ V, $V_{ds} = 10$ V. The plot is only shown for 0.1 μm distance from the AlGaN surface towards the substrate. (b) The conduction band profile corresponding to (a) but with $Q_{sp} = 0$.

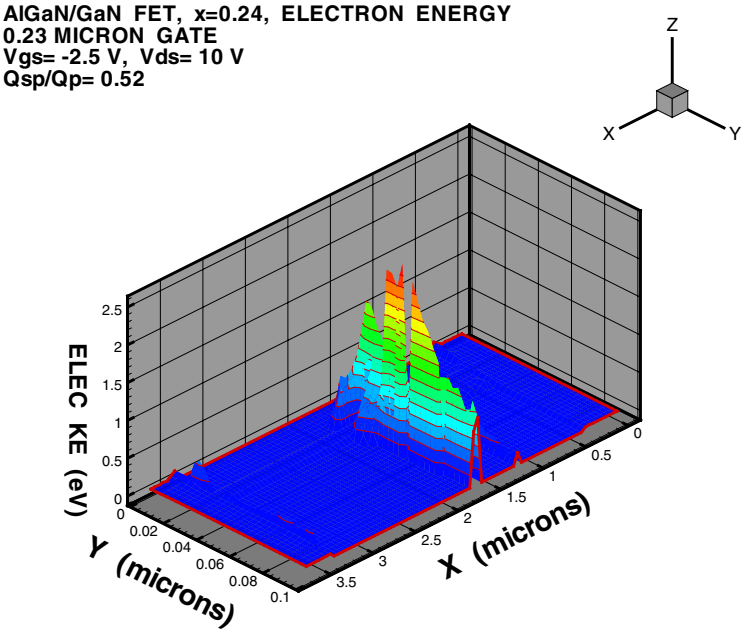

Figure 10. The profile of the mean kinetic energy for the simulation of figure 9(a). The potential drop at the drain edge of the gate generates the pulse of hot carriers with energy approaching 2 eV. These carriers diffuse into the AlGaN and towards the substrate.

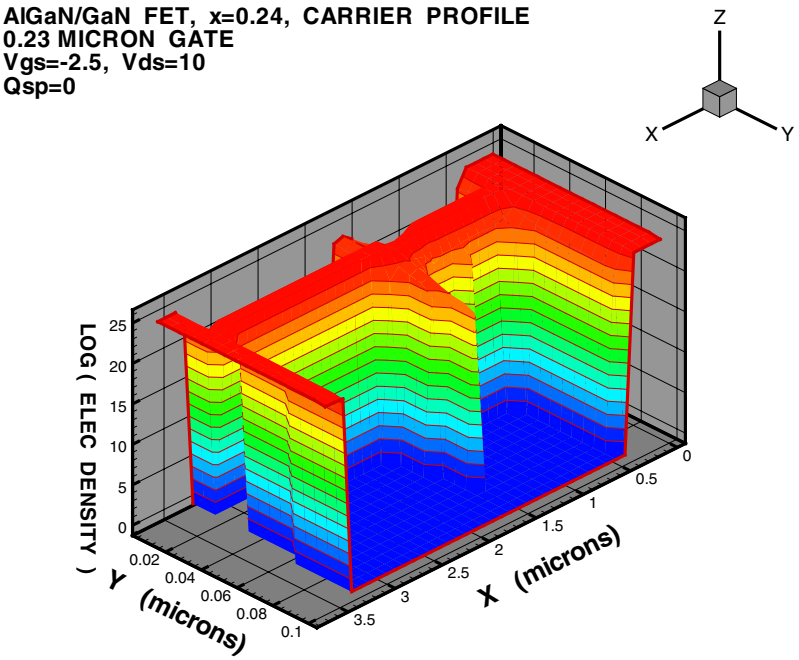

Figure 11. The profile of the electron density for the simulation of figure 9(b). The results show a well defined channel charge and diffusion of hot carriers into the AlGaN and towards the substrate. The positions of the device features are as described in figure 9(a).

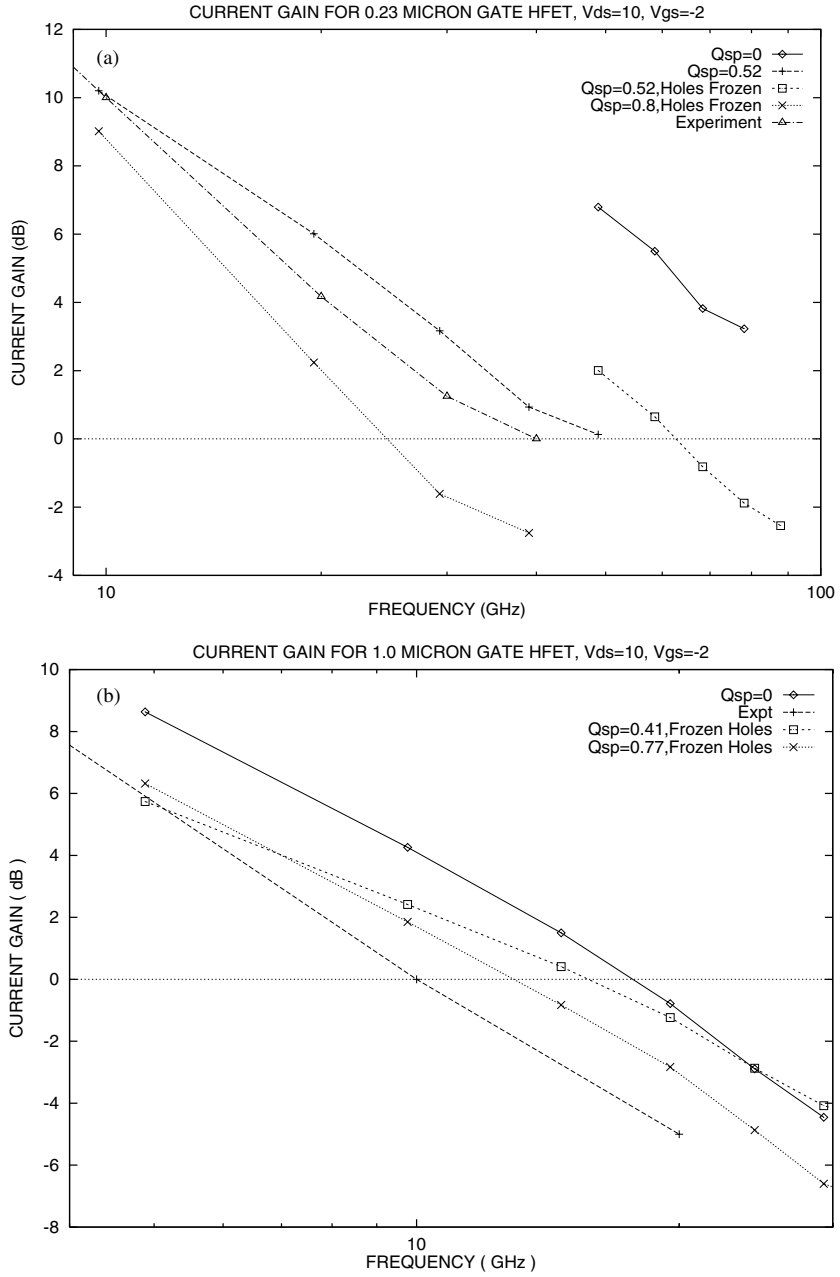

Figure 12. (a) The simulated high-frequency current gain for the 0.23 μm gate transistor. These results were obtained by using a dc bias of $V_{ds} = 10$ V, $V_{gs} = -2$ V and applying a small-signal pulsed voltage to the gate, with amplitude 0.2 V. A strong dependence of f_T on Q_{sp} is observed. Results obtained with both the mobile-hole and the frozen-hole models are shown. The latter bracket the experimental data. The decibel unit is defined as $20 \log_{10}(I_d/I_g)$. (b) A similar simulation to that in (a) but for the 1 μm gate transistor. The results in this case are less sensitive to Q_{sp} and are obtained with both the mobile- and frozen-hole models.

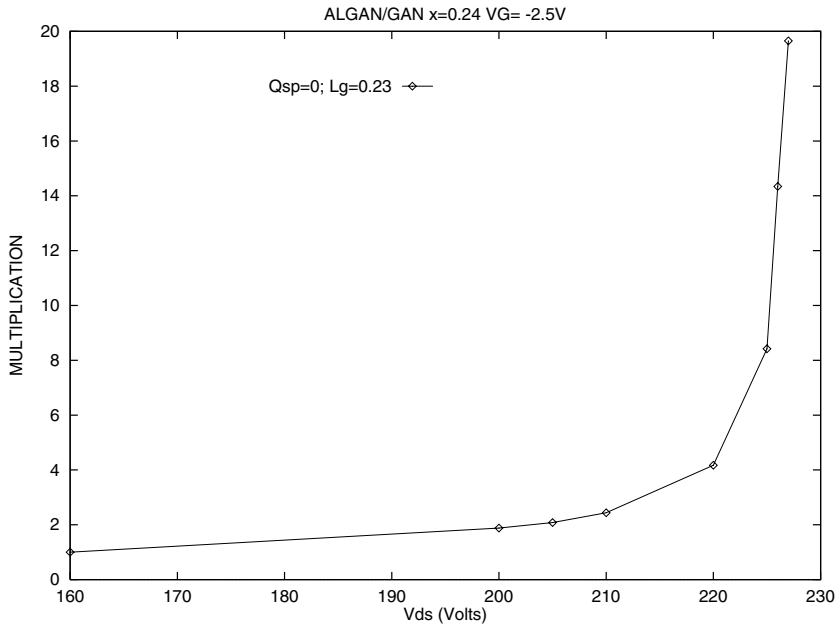

Figure 13. The carrier multiplication for a 0.23 μm gate HFET. Multiplication becomes significant for $V_{ds} > 200$ V.

the method described by Crow and Abram [16], the voltage pulse was taken to have a sinc form with an amplitude of 0.2 V. The simulations used time steps of 4×10^{-15} s and the output currents were averaged over 0.1 ps before Fourier transformation. The resulting current gain $I_d(\omega)/I_g(\omega)$ was then computed and the cut-off frequency f_T determined from the unit-current-gain frequency. In practice the Fourier-transformed currents were quite noisy and a smoothing routine was employed to obtain smooth curves which could be used to predict f_T.

Figure 12 shows the computed current gain for the two example transistors, assuming a lattice temperature of 300 K. In figure 12(a) the 0.23 μm gate transistor is predicted to have an f_T of about 100 GHz with a neutral AlGaN surface ($Q_{sp} = 0$), but this is reduced to about 42 GHz with $Q_{sp} = 0.52Q_p$ assuming mobile holes at the AlGaN surface. The experimental f_T for the transistor with a 0.2 μm gate is 38 GHz. The measurements are not pulsed, so lattice heating to about 350–400 K is likely. This will reduce the carrier velocity by about 10% if the temperature dependence is estimated from figure 3. Figure 12(a) also includes some results obtained by freezing the holes at the dc bias point. For $Q_{sp} = 0.52Q_p$, it is seen that freezing the holes leads to an increase in f_T, demonstrating that the mobile holes act to screen the signal potential and reduce the current gain. By increasing Q_{sp} to $0.8Q_p$ and freezing the holes, f_T is greatly reduced. The two values for f_T obtained with the frozen-hole model span the experimental measurements, showing that, in principle, reasonable values can be chosen to agree with experiment. For the 1 μm gate transistor in figure 12(b), the predicted cut-off frequencies using mobile holes are 18 GHz ($Q_{sp} = 0$) and 15 GHz ($Q_{sp} = 0.41$). Curves obtained with the frozen-hole model yield f_T-values of 16 GHz ($Q_{sp} = 0.41$) and 13 GHz ($Q_{sp} = 0.77$), which compares with an experimental value of 9.5 GHz.

From these results we conclude that the short-gate-length, high-speed transistors will be particularly sensitive to the charge state of the surface and that the potential experimental high-frequency performance is probably not being realized at present, because of the effects

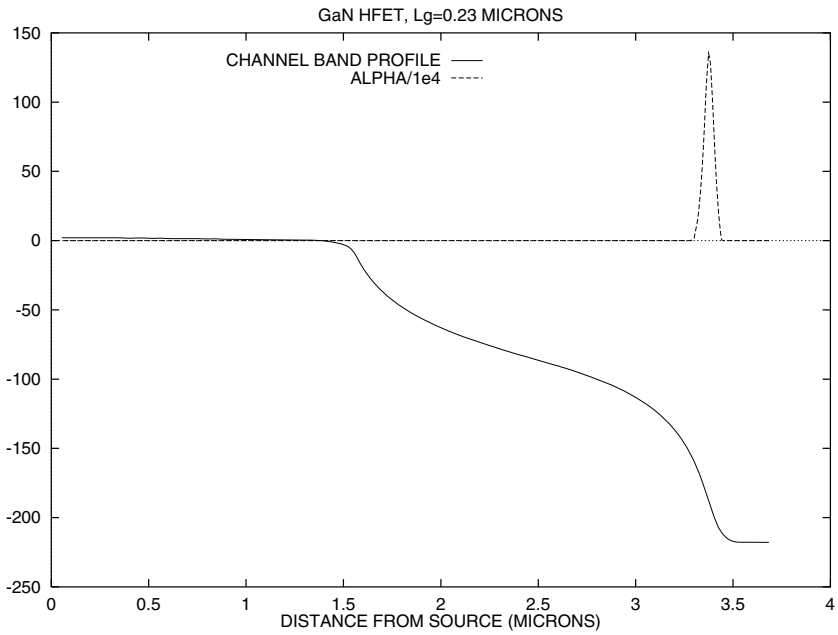

Figure 14. The band profile and electron ionization coefficient plotted along the GaN/AlGaN interface corresponding to the multiplication in figure 13 at $V_{ds} = 220$ V. Two high-field regions are shown between the gate and drain with band curvature corresponding to excess positive and excess negative charge. The potential is measured in volts and the electron ionization coefficient (alpha) in cm^{-1}. Alpha has been reduced by a factor of 10^4 in order to fit it into the plot.

of defects or surface charge. The comparison of theory and experiment is encouraging and suggests that our surface charge model may be on the right lines.

5. Breakdown

To study the breakdown characteristics of the transistors, we used the electron ionization coefficients measured in [4]. From the band profiles in figure 9 or the electron kinetic energy profiles in figure 10 we expect ionization to occur in the high-field regions between the gate and drain. To compute the breakdown voltage we used the potential profile and the associated electric field profile along the GaN/AlGaN interface between source and drain as obtained from SLURPS, and input the field profile into a separate computer code for calculating impact ionization. The measured ionization coefficients were used with the simple dead-space model developed by Tan *et al* [13] and a hard threshold in order to compute the carrier multiplication. The dead space was determined by setting the threshold energy for ionization equal to the real band gap of GaN, and is not affected by our use of a reduced band gap to model the deep acceptors. The calculation of ionization was not performed self-consistently, so can only give an approximate description of the breakdown characteristics. A fully self-consistent calculation allowing for trapping of the generated holes, with the consequent build-up of space charge, could be very interesting for determining the softness of the breakdown characteristics, but has not been attempted at this stage.

Figure 13 shows the multiplication values obtained for a 0.23 μm gate transistor assuming that $Q_{sp} = 0$. It is seen that the ionization becomes significant for $V_{ds} > 200$ V. If the surface

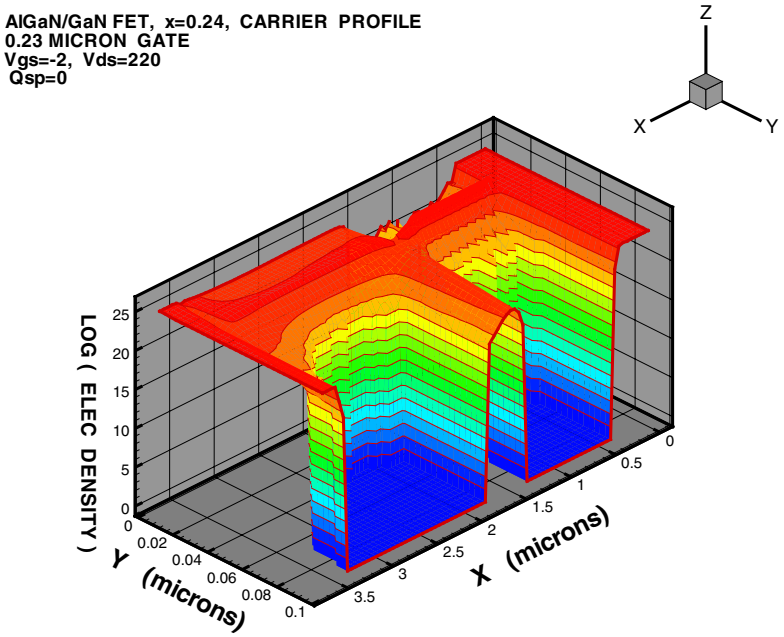

Figure 15. A profile of the electron density corresponding to figures 13 and 14. The geometry is the same as for figure 11. By comparison with figure 11, which represents the low-drain-voltage case, we see that at high voltage the hot-carrier lateral diffusion is considerably enhanced, both into the AlGaN and towards the substrate. A particularly interesting feature is the accumulation of carriers in the AlGaN close to the drain contact, which is related to the high-field region close to the drain in figure 14.

charge $Q_{sp} = 0.52Q_p$ is allowed for, then a multiplication of 20 is obtained at $V_{ds} = 150$ V, indicating that the breakdown voltage is sensitive to the surface condition. The corresponding band profile is shown in figure 14 plotted along the channel with the source at the origin. The band profile shows two regions of high electric field. The first region occurs at the drain end of the gate and is also observed at low drain voltage. This is caused by the high electron velocity and lateral diffusion of hot carriers, which reduces the electron density and exposes the positive charge of the channel polarization and the ionized donors in the AlGaN. The other high-field region occurs at the edge of the drain contact doping. The simulation results in figure 15 show reduced lateral diffusion of electrons towards the substrate in this second region and an increased concentration of electrons in the AlGaN layer. The curvature of the band profile indicates excess positive charge near the gate and excess negative charge near the drain. The latter may be explained by the electron accumulation in the AlGaN. Figure 14 also shows a plot of the electron ionization coefficient (rate per cm) for an electron flowing along the channel close to the GaN/AlGaN heterojunction, and it predicts that the ionization comes predominantly from the second high-field region close to the drain where the field is highest.

6. Conclusions

Self-consistent Monte Carlo simulations of GaN/AlGaN transistors have shown reasonable agreement with experimental data. The model has used ionization measurements to determine the magnitude of the inter-valley scattering rates. The polarization charge (Q_p) at the

AlGaN/GaN interface was obtained by fitting the experimental pinch-off voltage, and the p-doping level in the GaN was determined from substrate bias measurements. The relatively high drain currents and f_T-values obtained from the simulations for the (0, 0) quiescent bias, using a charge-neutral AlGaN surface, are probably caused by the relatively high drift velocity resulting from neglect of defect scattering processes which will be present in the material. A small overestimate of Q_p also contributes, as does contact resistance and gate de-biasing at the higher drain currents. The results suggest that a factor-of-two improvement in f_T may be possible with improving material quality.

In this paper we have given some preliminary results for a new model of deep levels at the AlGaN surface, in which only a fraction of the surface polarization charge is neutralized. The remainder (Q_{sp}) is treated as equivalent to a sheet of deep acceptor levels with holes which are mobile but with very low mobility. It was possible to obtain good agreement with experimental I_d–V_g data pulsed from the (0, 0) quiescent bias point by assuming that surface holes are mobile on the timescale (μs) of the experiments. This model, however, appears to be inconsistent with measurements of surface leakage current. Preliminary calculations with the alternative model in which holes in surface trap states are frozen at the dc quiescent bias show the expected trends of reducing I_d and f_T for quiescent bias points with high V_{gs} or V_{ds}. The high-quiescent-bias states expose the surface charge Q_{sp} and this influences the band profile and channel charge. Introducing large values for Q_{sp} at the (0, 0) quiescent bias, however, yields only small changes in the I_d-values obtained from the neutral-surface ($Q_{sp} = 0$) model. This indicates that surface trapping is unlikely to explain the high theoretical I_d, and the explanation in terms of neglected defect scattering appears to be more plausible. The frozen-hole model can lead to large current-slump effects. Further work is required to establish whether this model can explain the detailed current-slump data.

The model has also been used for some preliminary studies of the breakdown voltage, where values in excess of 200 V are predicted for $Q_{sp} = 0$ on a 0.23 μm gate transistor with $L_{gd} = 1.84$ μm. By using $Q_{sp} = 0.52Q_p$, the breakdown voltage is reduced to about 150 V. These values may be compared with a value of 170 V which has been reported for transistors with gate-to-drain separation of 2.0 μm [14]. The Monte Carlo simulations have also revealed interesting 2D structure of the breakdown phenomena, related to lateral hot-carrier diffusion, and this is an area requiring further theoretical study. The model of the AlGaN surface charge state looks promising but is at a preliminary stage and will be examined further in future work. Further simulations of pulsed data, examining current-slump effects by freezing the hole motion, should provide a severe test for the model of surface trapping.

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